REMARKS

Claim Rejections Under 35 U.S.C. § 103

Claims 1-3, 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Chuang et al.* (U.S. Patent No. 6,031,757) in view of *James, Jr. et al.* (U.S. Patent No. 6,240,519). Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Chuang et al.* in view of *James, Jr. et al.* as applied to claim 1 above, and further in view of *Kynett et al.* (U.S. Patent No. 5,249,158). Claims 6-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Chuang et al.* in view of *James, Jr. et al.* as applied to claim 1 above, and further in view of *Johnson et al.* (U.S. Patent No. 5,343,437). Applicants respectfully traverse this rejection.

Claims 1, 2, 5, 6, and 8 have been amended to more clearly claim the subject matter that Applicants regard as the invention. Claims 7 and 9 have been canceled without prejudice to avoid duplicate claiming.

Chuang et al. disclose a write protected, non-volatile memory device. *Chuang et al.* use a sector lock bit to lock protectable sectors of the device. *Chuang et al.*, however, neither teach nor suggest a memory device with boot blocks at most and least significant memory sectors. Nor do *Chuang et al.* teach or suggest loading memory protect status bits from a non-volatile register to a corresponding volatile register at power-up of the memory device as claimed in the presently amended claims.

Johnson et al. disclose memory having nonvolatile and volatile memory banks. A memory transfer circuit transfers the contents of a bank of nonvolatile memory array to a bank of volatile memory array before the data can be accessed by a processor. The Examiner states that it would have been obvious to combine the teachings of *Johnson et al.* with *Chuang et al.* since volatile memories are faster than non-volatile memories. However, since the present claims are to protecting and authorizing the erase of boot blocks of non-volatile memory devices, the slight speed difference between accessing a volatile register and accessing a non-volatile register is irrelevant.

It is well known in the art that erasing a non-volatile device is measured in at least milliseconds and more typically seconds whereas access times for non-volatile devices is typically measured in tens of nanoseconds. A volatile memory device can be accessed in nanoseconds. Therefore, the desirability of saving a few nanoseconds (or even tens of

nanoseconds) by accessing a protect bit in volatile memory versus non-volatile memory would be lost once the boot blocks are authorized to be erased. Thus, there is no desire or suggestion to combine the teachings of *Johnson et al.* with that of *Chuang et al.*, as suggested by the Examiner, and therefore it would not have been obvious to combine the two references.

Johnson et al. also neither teach nor suggest that a non-volatile register has a corresponding volatile register to which the data is loaded, as claimed in the amended claims of the present invention. *Johnson et al.* simply state that a preload circuit may transfer a bank of nonvolatile memory into volatile memory invisible to the processor (see Abstract).

James, Jr. et al. disclose an apparatus and a method to prompt for an administrative password during a boot block process. *James, Jr. et al.* further disclose first and second boot block sectors. However, *James, Jr. et al.* neither teach nor suggest these sectors being at most and least significant memory sectors of the memory array as claimed in the present claims. *James, Jr. et al.* also neither teach nor suggest loading a memory protect status bit from a non-volatile register to a volatile register during power-up nor is there a desire or suggestion to use a memory protect status bit.

Kynett et al. disclose flash memory blocking and a flash memory device with boot blocks at either the bottom end or the top end of the address space. *Kynett et al.*, however, neither teach nor suggest Applicants' invention as claimed in the amended claims for transferring a protect status bit from a non-volatile register to a corresponding volatile register at power-up of the memory device. In fact, *Kynett et al.* neither teach nor suggest protecting either boot block area as claimed in the amended claims of the present invention.

Applicants invention, as claimed in the amended claims, is to a memory device having boot block areas located at most and least significant memory areas. A protect status bit is transferred from a non-volatile register to a corresponding volatile register at power-up and this bit, along with a security voltage, is used to determine whether one of the boot blocks is protected from an erase operation. Applicants have shown that it would not have been obvious to combine the cited references since there is no desire or suggestion to combine.

CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

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